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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/773,224	02/09/2004	Taiji Noda	740756-1048	6741

22204 7590 04/26/2005

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EXAMINER	
SARKAR, ASOK K	

ART UNIT	PAPER NUMBER
2891	

DATE MAILED: 04/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/773,224	NODA, TAIJI	
	Examiner	Art Unit	
	Asok K. Sarkar	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-6,14 and 16-31* is/are pending in the application.

4a) Of the above claim(s) *16-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-6 and 14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *09 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☒ Certified copies of the priority documents have been received in Application No. 09/865,546.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi, US 5,134,452 in view of Burr, US 6,093,951 and Kizilialli, US 5,821,147.

Yamaguchi teaches a method for fabricating a semiconductor device having a MIS transistor comprising the steps of:

- preparing an epitaxial semiconductor substrate (as shown in Fig. 10B) with a multi-layer structure having an epitaxial region formed by epitaxial growing silicon 22 on a silicon substrate 1 in column 8, lines 5 – 22;
- forming a gate electrode 5 above said epitaxial region with a gate insulating film 4 sandwiched therebetween with reference to Fig. 8; and
- forming a diffusion layer 3 of said MIS transistor in said epitaxial region, by

using a dopant ion, wherein said diffusion layer is formed shallower than said epitaxial region with reference to Fig. 9.

Yamaguchi fails to teach diffusion layer formed by using a indium ion at a dose of 5×10^{13} cm^{-2} or more.

Burr teaches forming a FET device in which diffusion layers are formed by using In dopant having relatively small diffusion coefficient thereby forming pockets having steep concentration profile for the benefit of forming low threshold devices having a retrograde pocket region in column 14, lines 35 – 41.

Kizilialli teaches that In ion is implanted at a dose of 5×10^{13} cm^{-2} or more in column 1, lines 55 – 58 for the benefit of providing superior short channel behavior due to lower diffusion coefficient that minimizes diffusion of ion during thermal treatment in column 2, lines 5 – 11.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Yamaguchi and form the diffusion layers by indium ion at a dose of 5×10^{13} cm^{-2} or more for the benefit of forming low threshold devices having a retrograde pocket region as taught by Burr in column 12, lines 27 – 59 and also for the benefit of providing superior short channel behavior due to lower diffusion coefficient that minimizes diffusion of ion during thermal treatment as taught by Kizilialli in column 2, lines 5 – 11.

4. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi, US 5,134,452 in view of Burr, US 6,093,951 and Kizilialli, US 5,821,147 as applied to claim 1 above, and further in view of Koyama, US 5,177,569.

Burr and Kizilialli teach implanting In ion as was discussed previously in rejecting claim 1.

Burr and Kizilialli fail to teach epitaxial region having <110> - oriented zone axis.

Koyama teaches the advantages of dopant implantations in single crystal (110) plane orientation in between column 6, line 63 and column 7, line 24.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the diffusion layer in Burr's device with In and replace the substrate having <110> - oriented zone axis so that the epitaxial layer is formed with <110> - oriented zone axis since the transistor characteristics will be further enhanced as taught by Koyama in addition to being enhanced by using heavy weight dopant In.

5. Claims 4 – 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yamaguchi, US 5,134,452 in view of Burr, US 6,093,951 and Kizilialli as applied to claim 1, and further in view of Arai, US 5,972,783.

Regarding claims 4 and 14 Yamaguchi fails to teach the step of the forming the diffusion layer as pocket diffusion layer and form the said pocket diffusion layers on both sides of the gate by implanting a first dopant of a first conductivity type corresponding to said dopant ion into said epitaxial region with the gate electrode used as a mask; and forming an extension diffusion layer by implanting a second dopant of a second conductivity type into said epitaxial region to have shallower junction than said pocket diffusion layer with said gate electrode used as a mask.

Burr teaches the step of the forming the diffusion layer as pocket diffusion layer and form the said pocket diffusion layers on both sides of the gate by implanting a first

dopant of a first conductivity type corresponding to said dopant ion into said epitaxial region; and forming an extension diffusion layer by implanting a second dopant of a second conductivity type into said epitaxial region to have shallower junction than said pocket diffusion layer with references to Figs 5G – 5I in descriptions under column 14. Burr uses extra mask in addition to using gate electrode as a mask.

Kizilialli, however, uses gate electrode as a mask for implantation as shown in Figs 1, 3 and 4.

Arai teaches a method of fabricating a semiconductor device where he forms the pocket diffusion layer on both sides of the gate using it as a mask and the extension diffusion layer using the gate as a mask for the benefit of providing an improved punchthrough breakdown voltage in column 21, lines1 – 3.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Yamaguchi in view of Burr and Kizilialli to provide forming the pocket diffusion layer and the extension diffusion layer for the benefit of providing an improved punchthrough breakdown voltage as taught by Arai in column 21, lines1 – 3.

Regarding claim 5, Burr teaches forming the forming a channel diffusion layer by implanting a third dopant of the first conductivity type into said epitaxial region before forming the gate electrode with reference to Fig. 5B in column 13, lines 12 – 20.

Regarding claim 6, Burr teaches second dopant as Sb ion in column 14, lines 42 – 40.

6. Claims 1, 4 – 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bulucca, US 6,559,804 in view of Burr, US 6,093,951; Kizilialli, US 5,821,147 and Yamaguchi, US 5,134,452.

Regarding claim 1, Bulucca teaches a method for fabricating a semiconductor device having a transistor comprising the steps of:

- preparing an epitaxial semiconductor substrate with a multi-layer structure having an epitaxial region 50p formed by epitaxial growing silicon on a silicon substrate 200 (see Fig. 16 a) in column 34, lines 26 – 40;
- forming a gate electrode 68 above said epitaxial region with a gate insulating film 66 sandwiched therebetween (see Fig. 9a and 13a); and
- forming a diffusion layer 60M, 60E and 100 of said transistor in said epitaxial region (see Fig. 9a and 13a), by using In as a dopant ion (column 4, lines 46 – 52) wherein said diffusion layer is formed shallower than said epitaxial region (see Fig. 9a and 13a).

Bulucca fails to disclose forming all diffusion regions; using indium ion at a dose of 5×10^{13} cm^{-2} or more and the transistor device is a MIS transistor.

Burr teaches forming a FET device in which diffusion layers are formed by using dopant ion In or Sb of relatively large mass numbers and having relatively small diffusion coefficient thereby forming pockets having steep concentration profile for the benefit of forming low threshold devices having a retrograde pocket region in column 12, lines 27 – 59.

Kizilialli teaches that In ion is implanted at a dose of 5 x 10^{13} cm^{-2} or more in column 1, lines 55 – 58 for the benefit of providing superior short channel behavior due to lower diffusion coefficient that minimizes diffusion of ion during thermal treatment in column 2, lines 5 – 11.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to modify Bulucca and form the diffusion layers by indium ion at a dose of 5 x 10^{13} cm^{-2} or more for the benefit of forming low threshold devices having a retrograde pocket region as taught by Burr in column 12, lines 27 – 59 and also for the benefit of providing superior short channel behavior due to lower diffusion coefficient that minimizes diffusion of ion during thermal treatment as taught by Kizilialli in column 2, lines 5 – 11.

Yamaguchi teaches that MOSFET and MISFET are similar devices with an oxide film as an insulator (see column 1, lines 12 – 20). Bulucca teaches using oxide as a gate insulator with respect to Fig. 17 and therefore, Bulucca's device is also a MISFET device.

Regarding claims 4 – 6, Bulucca in view of Burr teaches limitations of these claims with respect to Figs. 9A and 13A.

Regarding claim 14, Bulucca teaches forming pocket diffusion layer 60E on both sides of the gate electrode 68 with respect to Figs. 9A and 13A.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bulucca, US 6,559,804 in view of Burr, US 6,093,951; Kizilialli, US 5,821,147 and Yamaguchi,

US 5,134,452 as applied to claim 1 above, and further in view of Koyama, US 5,177,569.

Bulucca in view of Burr, Kizilialli and Yamaguchi fails to teach epitaxial region having <110> - oriented zone axis.

Koyama teaches the advantages of dopant implantations in single crystal (110) plane orientation in between column 6, line 63 and column 7, line 24.

Therefore, it would have been obvious to one with ordinary skill in the art at the time of the invention to form the diffusion layer in Burr's device with In and replace the substrate having <110> - oriented zone axis so that the epitaxial layer is formed with <110> - oriented zone axis since the transistor characteristics will be further enhanced as taught by Koyama in addition to being enhanced by using heavy weight dopant In.

Response to Arguments

8. Applicant's arguments filed March 4, 2005 have been fully considered but they are not persuasive. The first part of the Applicant's argument (3rd paragraph, page 9) deals with the fact that Yamaguchi discloses a solid phase epitaxial layer instead of the Applicant's epitaxial growing silicon. The claim limitation cites "epitaxial growing silicon". The claim does not cite how the silicon was made such as vapor phase or liquid phase or for that matter, the solid phase. Since, the claim does not actually cite the method, the Examiner considers the epitaxial silicon as any epitaxial silicon, no matter how it was made. Therefore, Applicant's argument regarding disqualifying Yamaguchi as not being a valid reference is not found to be persuasive.

Regarding the Applicant's other argument with respect to the indium implantation

dose, Kizilialli, US 5,821,147 was used for the current Office Action that shows the implant dose cited in claim 1. Additionally, the Examiner reminds the Applicant, that Burr's dose, although sufficient for the boron dopant, may need to be increased to higher level for In, since, the diffusion coefficient of In is smaller than that of B and will therefore require higher dose to get the appropriate dopant concentration for Burr's device.

Conclusion

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Asok K. Sarkar whose telephone number is 571 272 1970. The examiner can normally be reached on Monday - Friday (8 AM- 5 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, William B. Baumeister can be reached on 571 272 1722. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

11. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Asok Kumar Sarkar

Asok K. Sarkar
April 22, 2005

Primary Examiner